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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/078,732 | 02/19/2002 | Kenneth Hing Key Tseng | 07716P001 | 6289 |

27660 7590 11/21/2003

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| EXAMINER | |
|---|---|
| TAT, BINH C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 11/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/078,732 | TSENG, KENNETH HING KEY | |
| | Examiner | Art Unit | |
| | Binh C. Tat | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This office action is in response to application 10/078732 filed on 02/19/02.

Claims 1-29 remain pending in the application.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-29 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Takiguchi (U.S. Patent No. 5986463).

4. As to claim 1 Takiguchi teaches a buffer for noise rejection in a logic circuit comprising: an input node (fig 1, 2 element 15 and 9a-9b); an output node (fig 1, 2 element 15 and 9a-9b); a first inverter coupled to the input node, the first inverter having a first device size (fig 1, 2 element 15 and col 6 lines 40-63 and 9a-9b); a second inverter coupled to the first inverter and the output node, the second inverter having a second device size at least six times greater than the first device size (fig 1, 2 and 9a-9b col 1 lines 25-39 and col 2 lines 31-col4 lines29).

5. As to claim 2, Takiguchi teaches wherein the first and second inverters each comprise CMOS devices (see fig 9a-c and 10 col1 lines 56-col2 lines 12 and col 8 lines 31-67).

6. As to claim 3, Takiguchi teaches wherein the second device size is approximately ten times larger than the first device size (fig 1, 2 and 9a-9b col 1 lines 25-39 and col 2 lines 31-col4 lines29).

7. As to claim 4, Takiguchi teaches wherein a ratio of the first device size to the second device size is in a range between 1:8 and 1:22 (fig 1, 2 and 9a-9b col 1 lines 25-39 and col 2 lines 31-col4 lines29).

8. As to claim 5, 16 and 24 Takiguchi teaches extracting parametric information from a layout of the logic network (fig 1 4-7); analyzing the logic network to identify a crosstalk-induced glitch at a node of a signal path in the logic inetwork (fig 1 4-7 col 10 lines 13-42); inserting a buffer at the node that functions to suppress a magnitude of the crosstalk-induced glitch, the buffer including first and second inverters coupled in series, the first and second inverters respectively having a device size ratio of 1:6 or larger (fig 1, 2 and 9a-9b col 1 lines 25-39 and col 2 lines 31-col4 lines29).

9. As to claim 6 Takiguchi teaches wherein the parametric information includes capacitance and resistance along the signal path of the logic network (fig 1 4-7 and col 7 lines 35-60)

10. As to claims 7, and 20 Takiguchi teaches wherein the first and second inverters comprise CMOS devices (see fig 9a-c and 10 col1 lines 56-col2 lines 12 and col 8 lines 31-67).

11. As to claim 8, 21 and 28 Takiguchi teaches wherein the device size ratio is in a range between 1:8 and 1:22 (see fig 9a-c and 10 col1 lines 56-col2 lines 12 and summary).

12. As to claim 9, 22 and 29 Takiguchi teaches wherein the device size ratio is approximately 1:10 (see fig 9a-c and 10 col1 lines 56-col2 lines 12 and col 8 lines 31-67 and summary).

13. As to claim 10, 11, and 23 Takiguchi teaches wherein the parametric information further includes timing slack available at the node of the signal path (fig 1, 2 element 15 and col 6 lines 40-63 and 9a-9b); and wherein the buffer has an associated delay that is smaller than the timing

slack available at the node of the signal path (see fig 9a-c and 10 col1 lines 56-col2 lines 12 and col 8 lines 31-67 and summary).

*14.* As to claims 12, 13, 17 and 25 Takiguchi teaches wherein the node comprises an input of a logic state device, and wherein the logic state device comprises a flip-flop (see fig 1-3).

15. As to claims 14, 18 and 26 Takiguchi teaches wherein the logic state device comprises a latch (see fig 1-3).

*16.* As to claims 15, 19 and 27 Takiguchi teaches wherein the logic state device comprises a register (see fig 1-3).

***Conclusion***

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art Unit 2825
NovemberNovember 17, 20033